UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,493	06/14/2001	Pankaj K. Jha	0325.00482	7913

60909 7590 10/15/2008

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
PATEL, HARESH N	

ART UNIT	PAPER NUMBER
2454	

MAIL DATE	DELIVERY MODE
10/15/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/881,493	JHA, PANKAJ K.	
	Examiner	Art Unit	
	HARESH N. PATEL	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date. _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are subject to examination.

2. The claims 1-20 were rejected in the office action mailed dated 6/22/2007.

3. The office action dated 6/22/2007 was provided considering the BPAI decision dated 5/15/2007 to affirm the rejections on the copending application 09/881367, i.e., provisional double patenting application for which the applicant filed a terminal disclaimer dated 11/24/2004.

4. This application was abandoned on 12/27/2007, six months after the office action mailed dated 6/22/2007; and the abandonment was mailed on 1/10/2008.

5. The applicant's petition request to withdraw the abandonment for further prosecution was received on 1/7/2008, more than six months after the office action mailed dated 6/22/2007.

6. The request to revive this application has been granted dated 9/19/2008; the abandonment has been withdrawn, and this office action has been provided.

7. The claims 1-20 are amended with additional limitations on 1/7/2008, over the rejections of the claims of the office action mailed dated 6/22/2007.

8. The rejection to the claims 1-20 including additional limitations has been presented in this office action and this office action has been made final, necessitated by the applicant's amendment to the claims.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Amended claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa et al. 5,936,966 (Hereinafter Ogawa) in view of "Official Notice".

11. As per claims 1 and 10, Ogawa teaches an assembly (e.g., col., 3, lines 44 – 59, col., 4, line 65 – col., 5, line 22) comprising:

a database circuit (e.g., col., 6, lines 38 – 67) configured to store a plurality pointer values (e.g., col., 12, lines 41 – 49, col., 2, lines 5 – 14) for a plurality of first parameters (e.g., col., 4, line 65 – col., 5, line 22) defined by of a first network protocol associated with first network (e.g., col., 5, lines 11 – 15) wherein, one of said first parameters is associated with a corresponding one of said pointer values (e.g., col., 4, line 65 – col., 5, line 22);

and a processing circuit (e.g., col., 13, lines 26 –55) configured to (i) process a particular one of said parameters (e.g., col., 11, lines 58 – 67, col., 13, lines 15 – 21) in an incoming packet received by the assembly from the first network (e.g., col., 3, lines 44 – 59) in accordance with said corresponding pointer value (e.g., col., 13, lines 20 –55) to produce a second parameter for a second network protocol associated with a second network (e.g., col., 9, lines 7 – 24), and (ii) configured to present an outgoing packet (e.g., col., 8, lines 50 – 63) from said assembly to the second network (e.g., col., 9, lines 7 – 24) containing the second parameter (e.g., col., 9, lines 7 – 24),

a first circuit (e.g., col., 12, lines 41 – 49, col., 2, lines 5 – 14) configured to delineate a receive frame received (e.g., col., 4, line 65 – col., 5, line 22) from a first network having a first network protocol to produce incoming packet (e.g., col., 4, line 65 – col., 5, line 22);

a second circuit configured to (i) store plurality of pointer values for a plurality (e.g., col., 12, lines 41 – 49, col., 2, lines 5 – 14) of first parameters (col., 10, lines 3 – 48) defined by said first network protocol (e.g., col., 4, line 65 – col., 5, line 22) wherein, one of said first parameters is associated with a corresponding one of said pointer values (e.g., col., 4, line 65 – col., 5, line 22); (ii) process a particular one of said parameters (e.g., col., 9, lines 7 – 24) in said incoming packet in accordance with said corresponding pointer value (e.g., col., 12, lines 41 – 49, col., 2, lines 5 – 14) to produce a second parameter for a second network protocol associated with a second network (e.g., col., 9, lines 7 – 24) and (ii) present an outgoing packet (e.g., col., 8, lines 50 – 63) containing said second parameter (e.g., col., 9, lines 7 – 24),

a third circuit (e.g., col., 12, lines 41 – 49, col., 2, lines 5 – 14) configured to frame the outgoing packet (e.g., col., 8, lines 50 – 63) to present a transmit frame to a second network (e.g., col., 12, lines 41 – 49, col., 2, lines 5 – 14).

"Official Notice" is taken that both the concept and advantages of producing a second parameter that is defined by a second network protocol associated with a second network is well known and expected in the art. For example, Yusa et. al., 5,633,806 discloses these limitations, col., 3, lines 2 – 58. Wilford et. al. 6,687,247 discloses these limitations, col., 5, lines 12 – 43. Azadet et al. 2001/0034729 discloses these limitations, col., 3, lines 2 – 38. Ayyagari et al. 6,894,991 discloses these limitations, col., 4, lines 8 – 42. Cashman et al., 6,192,491, Cisco discloses usage of these well-known limitations, col., 2, 8. Bagchi et al., 6,882,634, Broadcom

Corporation, discloses usage of these well-known limitations, col., 10, 20. Trachewsky et al., 6,993,101, Broadcom Corporation, discloses usage of these well-known limitations, col., 10, 20. Hsu, Qualcomm, 7,031,666, discloses usage of these well-known limitations, col., 14. Mallory et al., 2002/0006136 discloses usage of these well-known limitations, paragraphs 111-115, 154-157. Holloway et al., 2002/0012343 discloses usage of these well-known limitations, paragraphs 111-115, 154-157. Ptasinski et al., 2002/0041570 discloses usage of these well-known limitations, paragraphs 111-115, 154-157. Mallory et al., 2002/0042836, discloses usage of these well-known limitations, paragraphs 113-117, 155-159. Ptasinski et al., 2002/0080886 discloses usage of these well-known limitations, paragraphs 111-115, 154-157. Cashman et al., 6,212,569, Cisco discloses usage of these well-known limitations, col., 2, 8. Note: The citation of these several references has been provided considering the prosecution of this case in which several supplemental office action with new SSP had been provided. The above several references are provided to expedite the prosecution of this case that also contain overlapping support for the limitations including the claimed assembly with functionality supporting first and second protocols, frames, packets, decoding, frame delineation, etc., as claimed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the well-known concept of producing a second parameter that is defined by a second network protocol associated with a second network with the teaching's of Ogawa in order to facilitate the usage of the above-mentioned circuits because the concept of usage of the producing a second parameter that is defined by a second network protocol associated with a second network would support specifying what type of the protocol should be used for conversion of the data received over the first network. The specifying of the network protocol

would enhance handling the packets in the second network protocol for the sending packets utilizing the second network protocol over the second network.

12. As per claim 2, Ogawa teaches the following:

the database circuit is further configured to store a plurality of offset values and a plurality of length values for said first parameters (e.g., col., 11, lines 58 – 67, col., 13, lines 15 – 21), one of the first parameters is further associated with both a corresponding one of said offset values and a corresponding one of said length values and said processing circuit (e.g., col., 4, lines 3 – 12, col., 4, lines 45 – 54) is further configured to partition said incoming packet (e.g., col., 12, lines 41 – 49, col., 2, lines 5 – 14) in accordance with at least one of said offset values and at least one of said length values (e.g., col., 11, lines 58 – 67, col., 13, lines 15 – 21) to extract said particular first parameter (e.g., col., 9, lines 27 - 65).

13. As per claim 3, Ogawa teaches the following:

an interface through which said offset values, said length values and said pointer values are downloaded for storage in said database circuit (e.g., col., 11, lines 58 – 67, col., 13, lines 15 – 21).

14. As per claim 4, Ogawa teaches the following:

a parsing circuit configured to partition said incoming packet (e.g., col., 4, lines 3 – 12, col., 4, lines 45 – 54)

a plurality of peripheral blocks (e.g., col., 11, lines 58 – 67, col., 13, lines 15 – 21) coupled to said parsing circuit (e.g., col., 12, lines 41 – 49, col., 2, lines 5 – 14) identified by the pointer values and configured to perform a plurality of processes involving said first parameters and an assembling circuit coupled to said peripheral blocks (e.g., col., 11, lines 58 – 67, col., 13, lines 15 – 21) and configured to generate said outgoing packet (e.g., col., 12, lines 41 – 49, col., 2, lines 5 – 14).

15. As per claim 5, Ogawa teaches the following:

database circuit is further configured to store both a second offset value (e.g., col., 3, lines 1 – 23), and a second length value for said second parameter as defined by a second network protocol (e.g., col., 4, lines 16 – 61).

16. As per claim 6, Ogawa teaches the following:

an interface connectable to at least one of the peripheral blocks located external to said assembly (e.g., col., 3, lines 41 - 57).

17. As per claim 7, Ogawa teaches the claimed limitations as rejected above. However, Ogawa does not specifically mention about the peripheral blocks being particular circuits.

"Official Notice" is taken that both the concept and advantages of providing the peripheral blocks are at least two circuits selected from a group of circuits including a content addressable memory circuit, a parity circuit, a first-in-first-out circuit, time to live circuit, content comparison counter circuit, a value swapping circuit, a stuffing de-stuffing circuit, a cyclic

redundancy checksum length construction generator circuit, synchronization circuit, a frame relay lookup circuit, a data link header error control connection identifier circuit, a protocol identification analysis circuit, a point-to-point protocol verification circuit, parameter discard circuit, and a buffer circuit is well known and expected in the art. For example, Yusa et. al., 5,633,806 discloses these limitations, col., 3, lines 2 – 58. Wilford et. al. 6,687,247 discloses these limitations, col., 5, lines 12 – 43. Azadet et al. 2001/0034729 discloses these limitations, col., 3, lines 2 – 38. Ayyagari et al. 6,894,991 discloses these limitations, col., 4, lines 8 – 42.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the concept of making the processing non-programmable with the teaching's of Ogawa in order to facilitate the usage of the above-mentioned circuits because the concept of usage of the above mentioned well-known circuits would support handling of the packet related information. The usage of the circuits would help processing information that is related to the packet.

18. As per claim 8, Ogawa teaches the following:

said peripheral blocks are configured to simultaneously processes a plurality of said first parameters (e.g., col., 6, lines 1 – 15).

19. As per claim 9, Ogawa teaches the following:

processing circuit is implemented as only hardware (e.g., col., **5**, lines 8 – 38, for further clarification, col., 1, lines 41-43, col., 5, lines 43 – 45).

20. As per claim 9, Ogawa teaches the following: processing circuit is implemented including hardware (e.g., col., 5, lines 8 – 38, for further clarification, col., 1, lines 41-43, col., 5, lines 43 – 45). However, Ogawa does not specifically mention about usage of the circuit being only hardware. "Official Notice" is taken that both the concept and advantages of providing usage of the circuit being only hardware is well known and expected in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include usage of the circuit being only hardware with the teachings of Ogawa in order to facilitate usage of the only hardware circuit because it would support handling pointers and parameters. The well-known use of only hardware circuit would enhance processing of the pointers and parameters faster as compared to hardware circuit that are not only hardware based. For example, Cashman et al., 6,192,491, Cisco discloses usage of these well-known limitations, col., 2, 8. Bagchi et al., 6,882,634, Broadcom Corporation, discloses usage of these well-known limitations, col., 10, 20. Trachewsky et al., 6,993,101, Broadcom Corporation, discloses usage of these well-known limitations, col., 10, 20. Hsu, Qualcomm, 7,031,666, discloses usage of these well-known limitations, col., 14. Mallory et al., 2002/0006136 discloses usage of these well-known limitations, paragraphs 111-115, 154-157. Holloway et al., 2002/0012343 discloses usage of these well-known limitations, paragraphs 111-115, 154-157. Ptasinski et al., 2002/0041570 discloses usage of these well-known limitations, paragraphs 111-115, 154-157. Mallory et al., 2002/0042836, discloses usage of these well-known limitations, paragraphs 113-117, 155-159. Ptasinski et al., 2002/0080886 discloses usage of these well-known limitations, paragraphs 111-115, 154-157. Cashman et al., 6,212,569, Cisco discloses usage of these well-known limitations, col., 2, 8.

21. As per claim 11, Ogawa teaches the following:

wherein said second circuit is further configured to store a plurality of offset values and a plurality of length values (e.g., col., 9, lines 1 – 23) for said first parameters and one of said first parameters is further associated with both a corresponding one of said offset values an a corresponding one of said length values (e.g., col., 5, lines 11 –24, col., 9, lines 41 - 57) and partition said incoming packet (e.g., col., 6, lines 16 – 61) in accordance with said offset values and said length values (e.g., col., 5, lines 11 –24, col., 9, lines 41 - 57) to extract said first parameters from said incoming packet (e.g., col., 3, lines 7 – 16).

22. As per claim 12, Ogawa teaches the following:

wherein said first circuit is further configured to provided a plurality of frame delineation methods (e.g, col., 8, lines 41 - 57, col., 6, line 62 - col., 7, line 24) for a plurality of network protocols (e.g., col., 4, lines 11-24, col., 6, lines 15 - 22, lines 44 - 54).

23. As per claim 13, Ogawa teaches the following:

further comprising an interface (e.g, col., 5, lines 41 – 57, col., 8, line 58 - col., 9, line 24) configured to permit a selection among said frame delineation methods (e.g, col., 4, lines 16 - 34, col., 6, line 62 - col., 7, line 24).

24. As per claim 14, Ogawa teaches the following:

said third circuit (e.g., col., 7, lines 11 -24, col., 2, lines 41 - 57, col., 8, line 58 - col., 9, line 24) is further configured to provided a plurality of framing methods (e.g., col., 4, lines 4 - 57, col., 6, line 62 - col., 7, line 24, col., 8, lines 54 -65) for a plurality of network protocols (e.g., col., 7, lines 11 -24, col., 6, lines 15 - 22, lines 44 - 54).

25. As per claim 15, Ogawa teaches the following:

further comprising an interface (e.g., col., 3, lines 41 - 57, figures 11 and 15, col., 8, line 58 - col., 9, line 24) configured to permit a selection among said framing methods (e.g., col., 5, lines 16 – 34, col., 6, line 62 - col., 7, line 24, col., 8, lines 54 - 65).

26. As per claim 16, Ogawa teaches the following:

said third circuit (e.g., col., 6, lines 11 - 24, col., 9, lines 41 - 57, figures 11 and 15, col., 8, line 58 - col., 9, line 24) is further configured to delineate a second receive frame (e.g., col., 3, line 50 - col., 4, line 14) from said second network (e.g., col., 2, lines 11 - 24, col., 3, lines 41 - 57, col., 6, lines 15 -22, lines 44 - 54) to produce a second incoming packet (e.g., col., 9, lines 28 - 41).

27. As per claim 17, Ogawa teaches the following:

said first circuit is further configured to frame (e.g., col., 5, lines 41 -57, col., 3, lines 51 - 67, col., 4, lines 50 - col., 5, line 14, col., 6, line 62 - col., 7, line 24) a second outgoing packet (e.g., col., 3, lines 11 - 24, col., 10 , lines 11 - 28) derived from said second incmong packet to present a second transmit frame (e.g., col., 6, lines 41 -57, col., 3, lines 51 - 67, col., 4, lines 50 - col., 5, line 14, col., 6, line 62 - col., 7, line 24) to said first network.

28. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa and "Official Notice" in view of Gabrick et al., 2002/0161802 (Hereinafter Gabrick).

29. As per claim 18, Ogawa teaches the claimed limitation as rejected under claim 10. Ogawa also discloses a plurality of framing circuits (e.g., col., 3, lines 44 – 66).

Ogawa does not specifically mention about usage of a corresponding one of the network protocols.

Gabrick discloses a concept of using a corresponding one of the network protocols (e.g., col., 3, lines 44 – 66).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ogawa with the teachings of Gabrick in order to facilitate usage of a corresponding one of the network protocols because the corresponding network protocol would support replicating and transferring information between two entities. The replication and transferring information would support providing information to the network device.

30. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa and "Official Notice" in view of Wilford et al. 6,687,247 (Hereinafter Wilford) and Gabrick.

31. As per claim 19, Ogawa teach the claimed limitation as rejected under claim 10.

However, Ogawa does not specifically mention about a plurality of de-framing circuits.

Wilford discloses a plurality of de-framing circuits (e.g., use of several circuits for deframing, col., 2, lines 59 – col., 3, line 18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ogawa with the teachings of Wilford in order to facilitate usage of a plurality of de-framing circuits means because the de-framing circuits would enhance the handling the information associated with the packet, and the packet related information would help enhance the software to process information for the assembly.

Ogawa and Wilford do not specifically mention about usage of a corresponding one of the network protocols.

Gabrick discloses a concept of using a corresponding one of the network protocols (e.g., col., 3, lines 44 – 66).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ogawa and Wilford with the teachings of Gabrick in order to facilitate usage of a corresponding one of the network protocols because the corresponding network protocol would support replicating and transferring information between two entities. The replication and transferring information would support providing information to the network device.

32. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa and "Official Notice" in view of Yanagihara et al. 5,899,578 (Hereinafter Yanagihara).

33. As per claim 20, Ogawa teach the claimed limitation as rejected under claim 10.

However, Ogawa does not specifically mention about a fourth circuit connected to the second circuit and configured process a select of the first parameters.

Yanagihara discloses a fourth circuit connected to the second circuit (e.g., two connected circuits that handle video data and audio data for processing, figure 10A, col., 1, lines 51 - 66) and configured process a select of the first parameters (e.g., processing of video data, audio data, broadcast programs etc., figure 10A, col., 1, lines 51 - 66).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ogawa with the teachings of Yanagihara in order to facilitate usage of a fourth circuit connected to the second circuit and configured process a select one of the first parameters because the another circuit would enhance the handling the information associated with the packet, and the packet related information would help enhance the software to process information for the assembly. The connection between two circuits would provide communication between two devices.

34. Considering the applicant's to the amendments to the independent claims 1, 10, with additional limitations; below are further rejections to demonstrate that the claimed subject matter is indeed not novel.

Claim Rejections - 35 USC § 102

35. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

36. Claims 1, 10, are rejected under 35 U.S.C. 102(e) as being anticipated by Ptasinski et al., 2002/0080886 (Hereinafter Ptasinski).

37. Referring to claim 1, Ptasinski discloses an assembly (e.g., assembly for frame delineation and encoding of parameters from one protocol to another protocol over different networks, page 5) comprising: a database circuit configured to store a plurality of pointer values for a plurality of first parameters defined by a first network protocol associated with a first network (e.g., page 5), wherein each one of said first parameters is associated with a corresponding one of said pointer values (e.g., page 5); and a processing circuit configured to (i) process a particular one of said first parameters in an incoming packet received by said assembly from the first network in accordance with said corresponding pointer value to produce a second parameter defined by a second network protocol associated with a second network (e.g., page 6) and (ii) present an outgoing packet from said assembly to the second network containing said second parameter (e.g., page 6).

38. Referring to claim 10, Ptansinki discloses an assembly (e.g., assembly for frame delineation and encoding of parameters from one protocol to another protocol over different networks, page 5) comprising: a first circuit configured to delineate a receive frame received from a first network having a first network protocol to produce an incoming packet (page 5); a second circuit configured to (i) stored a plurality of pointer values for a plurality of first parameters defined by said first network protocol (page 5), wherein each one of said first parameters is associated with a corresponding one of said pointer values (page 5), (ii) process a

particular one of said first parameters in said incoming packet in accordance with said corresponding pointer value to produce a second parameter defined by a second network protocol associated with a second network (page 6), and (iii) present an outgoing packet containing said second parameter; and a third circuit configured to frame said outgoing packet to present a transmit frame to the second network (page 6).

39. Claims 1, 10, are rejected under 35 U.S.C. 102(e) as being anticipated by Hsu, 7,031,666 (Hereinafter Hsu).

40. Referring to claim 1, Hsu discloses an assembly (e.g., col., 9) comprising: a database circuit configured to store a plurality of pointer values for a plurality of first parameters defined by a first network protocol associated with a first network (e.g., col., 9), wherein each one of said first parameters is associated with a corresponding one of said pointer values (e.g., col., 9); and a processing circuit configured to (i) process a particular one of said first parameters in an incoming packet received by said assembly from the first network in accordance with said corresponding pointer value to produce a second parameter defined by a second network protocol associated with a second network (e.g., col., 11) and (ii) present an outgoing packet from said assembly to the second network containing said second parameter (e.g., col., 11).

41. Referring to claim 10, Hsu discloses an assembly (e.g., col., 9) comprising: a first circuit configured to delineate a receive frame received from a first network having a first network protocol to produce an incoming packet (col., 9); a second circuit configured to (i) stored a

plurality of pointer values for a plurality of first parameters defined by said first network protocol (col., 9), wherein each one of said first parameters is associated with a corresponding one of said pointer values (col., 9), (ii) process a particular one of said first parameters in said incoming packet in accordance with said corresponding pointer value to produce a second parameter defined by a second network protocol associated with a second network (col., 11), and (iii) present an outgoing packet containing said second parameter; and a third circuit configured to frame said outgoing packet to present a transmit frame to the second network (col., 11).

Response to Arguments

42. Applicant's arguments filed 1/7/2008, pages 8-20, have been fully considered but they are not persuasive. Therefore, rejection of the claims 1-20 is maintained.

43. The applicant's statements, Applicant respectfully notes that in the Advisory Action mailed November 28, 2006, the Patent Office specifically indicated that "[t]he objections to the drawings, title, and the claims 1, 10, and 20 are withdrawn." [Advisory Action mailed November 28, 2006, page 2 on "Continuation Sheet"] A copy of the Advisory Action with the aforementioned statement highlighted is attached for the convenience of the Patent Office. Accordingly, in the next communication, Applicant respectfully requests that the Patent Office properly indicate that the aforementioned objections are withdrawn, are acknowledged. Hence, withdraw of these objections are again acknowledged.

Regarding the rejections of the claims, the applicant is kindly informed that the rejections are made using the cited arts, which is the evidence and the explanation regarding the evidence would not invalidate the evidence. The amending of the limitations of the claims to

overcome the rejections of the previously rejected claims has in fact narrowed the scope of the claimed subject matter. The office action dated 6/22/07 was provided considering the BPAI decision dated 5/15/2007 on the copending application 09/881367, i.e., provisional double patenting application for which the applicant has filed a terminal disclaimer dated 11/24/2004, and the BPAI decision that the limitations similar to the limitations of the claim 9 of this application under prosecution, is not disclosed by the Ogawa and well-known in the art, the finality of the rejection of the last Office action is withdrawn. To be consistent with the BPAI decision dated 5/15/2007, the claim 9 is no longer rejected under 35 U.S.C. 102(e) and is rejected under 35 U.S.C. 103(a) and hence this office action is made non-final. However, the claimed limitations have been amended over the rejections.

Regarding the applicant's concern, Ogawa is directed to a data receiving device that enables simultaneous execution of processes of a plurality of protocol hierarchies and generates header end signals. In particular, Ogawa teaches a sequencer 32 that is provided with a plurality of protocol processing circuits for independently carrying out at least a part of processes to respective protocol hierarchies of the protocol in response to sequence selection by a sequence selection circuit 28 according to a result of received protocol type identification in a protocol recognition circuit 26. [See Ogawa, Abstract]; Ogawa specifically teaches that the data receiving device 106 has an input data control circuit 22, a capture register circuit 24, a protocol recognition circuit 26, a sequence selection circuit 28, a sequence counter 30, a sequencer 32, a frame end detection circuit 34, a header end timing detection circuit 36, an interrupt generation circuit 38, and an external circuit 40. [See, e.g., Ogawa, Figure 1] ; Ogawa does not disclose database circuit, Therefore, it is respectfully submitted that Ogawa does not teach the feature of a

database circuit configured to store a plurality of pointer values for a plurality of first parameters defined by a first network protocol associated with a first network, wherein each one of said first parameters is associated with a corresponding one of said pointer values; the examiner respectfully disagrees. First the applicant has amended the limitations, which was neither proposed during the previous office actions nor required for any rejections. Note: the objections were withdrawn in the advisory action, which the applicant requested for re-clarification. The amended limitations are rejected under 35 U.S.C. 103(a) rejections. The relied upon disclosure and the teachings of the Ogawa are not limited as concluded by the applicant. Ogawa discloses the broadly claimed limitations, i.e., please see the cited portions among other places of the cited art that not only contain the applicant concerned content of the art but also the relied upon limitations. Further regarding the applicant's continued arguments even after amending the claimed limitations of the independent claims, to not further complicate the prosecution, please refer to the responses to the arguments (other than the claim 9) in the office action dated, 8/31/2006, office action 6/14/2006, and advisory office action dated 11/28/2006 after the interview summary dated 9/14/2006. The specification of the application under prosecution at pages 21-22 very clearly states, The function performed by the flow diagram of FIG. 4 may be implemented using a conventional general purpose digital computer programmed according to the teachings of the present specification, as will be apparent to those skilled in the relevant art(s). Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present disclosure, as will also be apparent to those skilled in the relevant art(s). The present invention may also be implemented by the preparation of ASICs, FPGAs, or by interconnecting an appropriate network of conventional component circuits, as is described

herein, modifications of which will be readily apparent to those skilled in the art(s). The present invention thus may also include a computer product which may be a storage medium including instructions which can be used to program a computer to perform a process in accordance with the present invention. The storage medium can include, but is not limited to, any type of disk including floppy disk, optical disk, CD-ROM, and magneto-optical disks, ROMs, RAMs, EPROMs, EEPROMs, Flash memory, magnetic or optical cards, or any type of media suitable for storing electronic instructions. While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention. Similarly, throughout the specification clarification for the alternate implementations are also mentioned. Further, when reviewing a reference the applicants should remember that not only the specific teachings of a reference but also reasonable inferences which the artisan would have logically drawn therefrom may be properly evaluated in formulating a rejection. **In re Preda, 401 F. 2d 825, 159 USPQ 342 (CCPA 1968) and In re Shepard, 319 F. 2d 194, 138 USPQ 148 (CCPA 1963).** Skill in the art is presumed. **In re Sovish, 769 F. 2d 738, 226 USPQ 771 (Fed. Cir. 1985).** Every reference relies to some extent on knowledge of persons skilled in the art to complement that which is disclosed therein. **In re Bode, 550 F. 2d 656, 193 USPQ 12 (CCPA 1977).**

Conclusion

44. Considering the BPAI decision dated 5/15/2007 on the copending application 09/881367, i.e., provisional double patenting application for which the applicant has filed a terminal

disclaimer dated 11/24/2004, the applicant is recommended, MPEP 1201 states: Where the differences of opinion concern the denial of patent claims because of prior art or other patentability issues, the questions thereby raised are said to relate to the merits, and appeal procedure within the Office and to the courts has long been provided by statute (35 USC 143). 35 U.S.C. 134 (a) states: An applicant for a patent, any of whose claims has been twice rejected, may appeal from the decision of the primary examiner to the Board of Patent Appeals and Interferences, having once paid the fee for such appeal.

45. In order to expedite the prosecution of this case, multiple references are used for the rejections to demonstrate that several references disclose the claimed subject matter of the claims. All the references including the "Official Notice" support references were part of the previously provided PTO-form 892's of the prosecution history.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Examiner has cited particular columns and line numbers and/or paragraphs and/or sections and/or page numbers in the reference(s) as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety, as potentially teaching, all or part of the claimed invention, as well as the context of the passage, as taught by the prior art or disclosed by the Examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Haresh Patel whose telephone number is (571) 272-3973. The examiner can normally be reached on Monday, Tuesday, Thursday and Friday from 10:00 am to 8:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached at (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Haresh N. Patel/

Primary Examiner, Art Unit 2154

9/19/2008